GP2123 #6 CB 02-26-02

PATENT
068167.0105

Pursuant to 37 C.F.R. § 1.8, I hereby certify that I have information and a reasonable basis for belief that this correspondence will be deposited as first-class mail with the United States Postal Service in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231.

Signature

1-17-02
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	
	§	
Traut, Eric P.	§	Group No.: 2123
	§	
Serial No.: 09/747,492	§	Examiner: Not Yet Assigned
	§	
Filed: December 21, 2000	§	
	§	
Invention: System and Method for the Logical Substitution of Processor Control in an Emulated Computing Environment	§	

Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

Applicant respectfully requests, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner. Pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

The information disclosure statement submitted herewith is being submitted before the mailing of the first office action on the merits. Applicants believe that no fee is required. If a fee is required, please charge any fee to Deposit Account No. 02-0383 of Baker Botts L.L.P.

Respectfully submitted,

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Date: January 17, 2002

PTO-1449

Information Disclosure Citation in an Application

Application No.	Applicant(s)		
09/747,492	Eric P. Traut		
Docket Number	Group Art Unit	Filing Date	
068167.0105	2123	12/21/00	

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	A	5278973	1/11/94	O'Brien et al.	395	500	6/27/91
	B	5301277	4/5/94	Kanai	709	301	12/23/91
	C	5367628	11/22/94	Ote et al.	345	501	10/15/92
	D	5448264	9/5/95	Pinedo et al.	345	508	6/14/93
	E	5452456	9/19/95	Mourey et al.	713	100	12/18/92
	F	5502809	3/26/96	Takano	345	509	9/6/94
	G	5640562	6/17/97	Wold et al.	395	652	2/27/95
	H	5666521	9/9/97	Marisetty	345	525	11/20/96
	I	5742797	4/21/98	Celi, Jr. et al.	345	507	8/11/95
	J	5752275	5/12/98	Hammond	711	207	7/14/97
	K	5757386	5/26/98	Celi, Jr. et al.	345	507	8/11/95
	L	5790825	8/4/98	Traut	712	209	8/5/97
	M	5831607	11/3/98	Brooks	345	333	1/25/96
	N	5860147	1/12/99	Gochman et al.	711	207	9/16/96
	O	5940872	8/17/99	Hammond et al.	711	207	11/1/96
	P	6014170	1/11/00	Pont et al.	348	232	6/20/97
	Q	6026476	2/15/00	Rosen	711	206	8/6/97
	R	6067618	5/23/00	Weber	713	1	3/26/98

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	
	S	"Processor Instruction Sets," The PC Guide, version date 12/18/00, http://www.pcguide.com/ref/cpu/arch/int/inst-c.html.	
	T	"M68060 User's Manual," Motorola, 1994, pp. i-xviii; Section 4, Memory Management Unit, pp. 4-1 to 4-30, http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/68K-COLDFIRE/M680X0/MC68060UM.pdf.	
	U	"MPC750, RISC Microprocessor User's Manual," Motorola, 8/97, Contents, pp. iii-xvi; Chapter 5, Memory Management, pp. 5-1 to 5-34; Glossary, pp. Glossary-1 to Glossary-13, http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/POWERPC/MPC7XX/MPC750UM.pdf.	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.